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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/823,148 | 04/13/2004 | Chrong Jung Lin | 252016-2330 | 4545 |

47390 7590 01/10/2006

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| EXAMINER | |
|---|---|
| SOWARD, IDA M | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2822 | |

DATE MAILED: 01/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

EIC

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/823,148 | LIN ET AL. | |
| | Examiner | Art Unit | |
| | Ida M. Soward | 2822 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *03 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *19-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19-22 and 24-32* is/are rejected.

7)☒ Claim(s) *23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

This Office Action is in response to the Applicants' amendment filed November 3, 2005.

### *Claim Rejections - 35 USC § 112*

The rejection to claim 21 under 35 U.S.C. 112, second paragraph, has been withdrawn due to the amendment filed.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 24 and 27-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Liang et al. (5,877,523).

In regard to claim 24, Liang et al. teach a multi-level, multi-bit stacked gate flash memory cell structure, comprising: two floating gates 18' & 18" on an insulating layer 16 on a substrate 12, having opposite sidewalls facing each other; a conformal dielectric layer 19 covering opposite sidewalls of the two floating gates 18' & 18"; a control gate 20 therebetween the opposite sidewalls of the two floating gates 18' & 18" with intervening the conformal dielectric layer 19; and two insulative spacers 28 covering

outside walls of the two floating gates 18' & 18" (Figure 8, columns 4-5, lines 18-67 and 1-52, respectively).

In regard to claim 27, Liang et al. teach the floating gates 18' & 18" and control gate 20 comprising polysilicon (Figure 8, columns 4-5, lines 18-67 and 1-52, respectively).

In regard to claim 28, Liang et al. teach the conformal dielectric layer 19 comprising oxide-nitride-oxide (ONO) (Figure 8, column 4, lines 50-67).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 19-22, 25-26 and 29-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liang et al. (5,877,523) in view of Sekariapuram et al. (6,091,102).

Liang et al. teach all mentioned in the rejection above.

In regard to claim 20, Liang et al. further teach said floating gate spacers 22 & 22' comprising polysilicon having a lateral thickness of 1500 Å, which is between about 500 to 2000 Å (column 3, lines 46-50).

However, Liang et al. fail to teach floating gate spacers having convex walls facing each other, and vertical outside walls; conformal dielectric layer covering said

convex walls of said floating gate spacers a control gate therebetween said convex walls of said floating gate spacers with intervening said conformal dielectric layer.

In regard to claim 19, Sekariapuram et al. teach floating gate spacers FG having convex walls facing each other, and vertical outside walls; conformal dielectric layer 126 covering said convex walls of said floating gate spacers FG a control gate CG therebetween said convex walls of said floating gate spacers FG with intervening said conformal dielectric layer 126 (Figure 1, column 5, lines 6-64).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the multi-level, multi-bit stacked gate flash memory cell structure as taught by Liang et al. with the multi-level, multi-bit stacked gate flash memory cell structure having floating gate spacers having convex walls facing each other, and vertical outside walls; conformal dielectric layer covering said convex walls of said floating gate spacers a control gate therebetween said convex walls of said floating gate spacers with intervening said conformal dielectric layer as taught by Sekariapuram et al. to improve operating characteristics (column 1, lines 29-38)

In regard to claim 22, Sekariapuram et al. teach the control gate CG comprising polysilicon (Figure 1).

In regard to claims 25 and 29, Sekariapuram et al. teach a first, second and third doped regions 112, 110 & 108 in the substrate 103 as source/drain regions, wherein the first doped region 112 is disposed between the two opposite sidewalls of the two floating gates FG, and the second and third doped regions 110 & 108 are disposed

outside of the outside walls of the two floating gates FG respectively (Figure 1, column 5, lines 6-64).

In regard to claims 26 and 30, Sekariapuram et al. teach the substrate 103 being a p-type semiconductor substrate and the first, second and third doped regions 112, 110 & 108 being n-doped regions, and the first n-doped region 112 serves as a source region and the second and third n-doped regions 110 & 108 serve as drain regions (Figure 1, column 5, lines 6-64).

### *Allowable Subject Matter*

Claim 23 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### *Response to Arguments*

Applicant's arguments with respect to claims 19-32 have been considered but are moot in view of the new ground(s) of rejection.

### *Conclusion*

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to multi-level, multi-bit stacked gate flash memory cells:

An et al. (6,051,470)

Hsieh (US 6,245,614 B2)

Johnson et al. (US 6,525,371 B2)

Kim et al. (US 6,803,276 B2)

Yang (US 6,329,248 B1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M. Soward whose telephone number is 571-272-1845. The examiner can normally be reached on Monday - Thursday 6:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra V. Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IMS
January 5, 2006

Ida M. Soward
AU 2822